

Innosilicon USB 2.0 OTG/Hub PHY

40nm/55nm/65nm/90nm/0.11um/0.13um

USB PHY
DATASHEET BRIEF

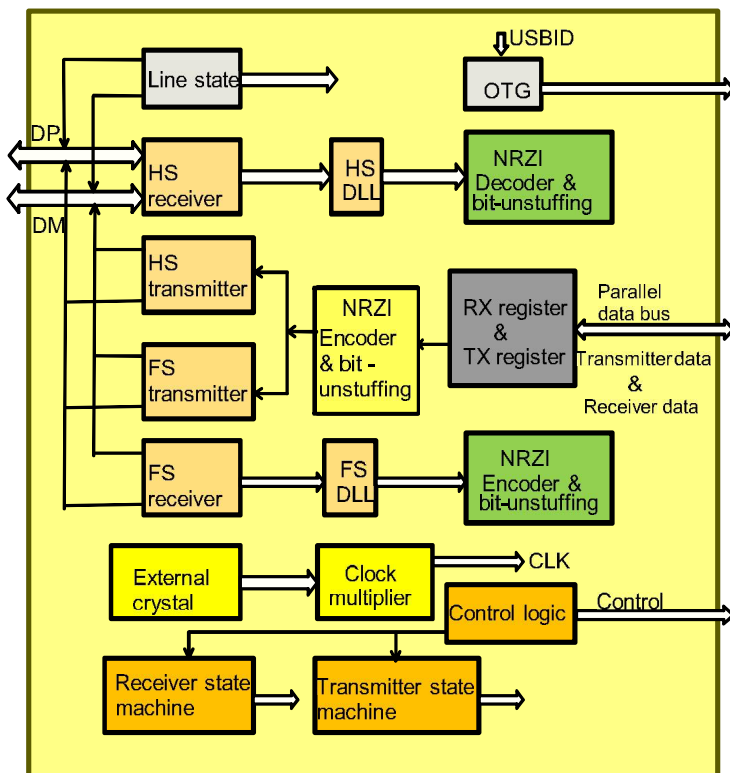
OVERVIEW:

The INNOSILICON USB2.0 Device / Host / OTG / Hub PHY conforms to the specification of UTMI+ level 3 Revision 1.0. As integrated high speed mixed signal circuits, The INNO USB2.0 PHY supports not only the High Speed (HS) traffic at 480 Mbps, the Full Speed (FS) traffic at 12Mbps and the Low Speed (LS), but also very low latency high speed and low speed Hub mode which has as low as 40 bit time round trip delay. The INNOSILICON Universal Serial Bus (USB) transceiver provides a complete range of peripheral functions. It is silicon proven and compliant with USB specifications version 2.0 as well as OTG supplements. It is available to be used as stand alone PHY or be part of USB3.0 solution which is coming soon.

MAJOR FEATURES :

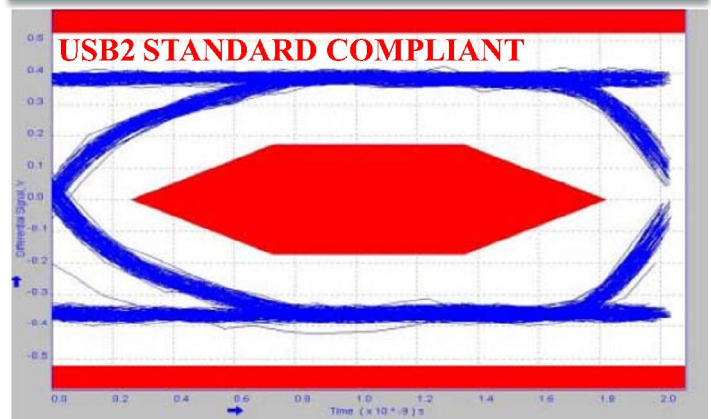
- Fully compliant with USB specifications Rev 2.0, 1.1 & OTG, Hub supplement
- Very small die size and low power
- Supports 480Mbps (HS), 12Mbps (FS)& 1.5Mbps (LS) serial data transmission
- Supports low latency hub mode with 40 bit time round trip delay
- Support very low latency hub mode
- 8 bit or 16 bit UTMI interface compliant with UTMI+ specification level 3 Rev 1.0
- Scan and Loop back BIST mode supported
- 12MHz crystal oscillator input
- 3.3V for analog transceiver power
- 1.0/1.2V for digital transceiver power
- Integrated phase-locked loop (PLL) oscillator
- Self-calibrated termination resistance
- Small die size
- SMIC 0.13um/0.11um/65nm/55nm/40nm and TSMC 65nm/55nm/40nm process
- Built-in I/O and ESD structure
- USB3.0 COMING, ASK US

BLOCK DIAGRAM:



KEY ADVANTAGE:

- Small die size, easy to integrate
- Low power consumption
- High speed hub use VLPI low latency
- Test chip and test board available
- FPGA integration Support



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