

Innosilicon SATA2/PCIE2/XAUI Multi-standard SERDES PHY IP

SERDES IP DATASHEET BRIEF

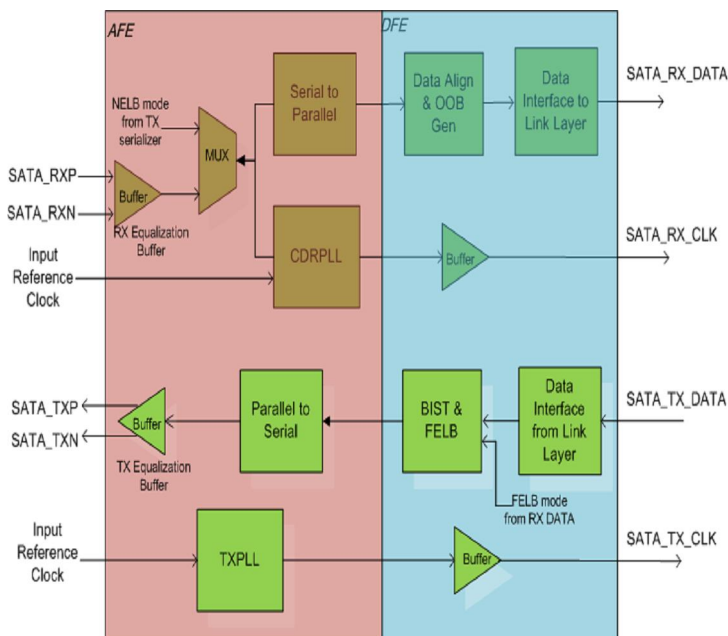
OVERVIEW:

The INNOSILICON mixed signal SATA2/PCIE2/XAUI-IP™ transceiver PHY provides a complete SATA2/PCIE/XAUI standard compliant transceiver physical interface solution for delivering high speed data over point to point link up to 6Gbps. It is optimized for high speed applications with robust timing and small silicon area in 40nm, 65nm, 90nm 0.13um process. For SATA2/PCIE2/XAUI-IP™ receiver, high speed interface clock and data recovery (CDR) processing equipped with tunable On-Die-Termination and equalization is available within the PHY to reliably capture transmit data in the center of the data eye

MAJOR FEATURES:

- Support SATA 3Gbps Gen 2 speed plus PCIe and XAUI up to 5Gbps
- Compliant with SATA2.0 specification, PCIE Gen2, and IEEE802.3ae XAUI.
- TX Drivers with tunable On-Die-Termination, programmable output swing, and pre-emphasis to ensure 600mV to 800mV signal window.
- Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Provide auto-calibrated on-die matched termination (differential).
- Embedded ESD, boundary scan support
- Extract data and clock from the serial stream with the aid of advanced jitter buffer.
- Detect the comma character and forward it to the Link Layer along with the 8/10, 16/20 or 32/40 bit wide parallel output
- SMIC 0.13um/65nm/55nm/40nm and TSMC 65/55nm/40nm
- SATA3.0 6Gbps Serdes in SMIC 65nm/55nm/40nm coming soon

BLOCK DIAGRAM:



KEY ADVANTAGES:

- Low Power
- Small Area
- Testchip and FPGA board support

APPLICATIONS:

- SATA2.0 /3.0 applications
- Portable hard disk
- High speed fiber/copper backplane
- PCIE applications

Visit our website at www.innosilicon.com for additional product information.

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