

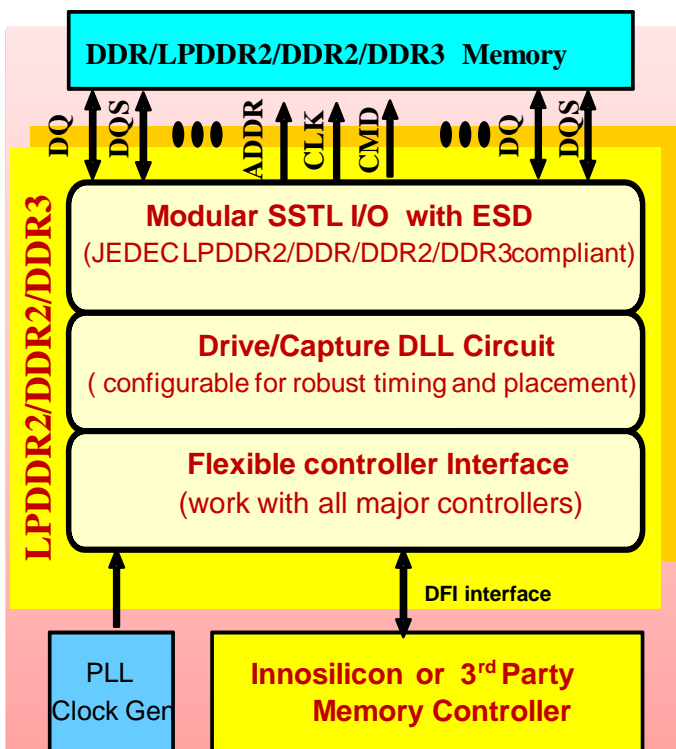
OVERVIEW:

This industry leading performance Mixed-Signal DDRn Combo PHYs provide the most advanced physical interface solutions for ICs requiring access to all sorts of JEDEC SDRAM devices. The PHY is production and SI simulation proven with low IO pin count and 2 layer PCB support. It comes with standard DFI V2.1 interface and is optimized for low power and high speed (up to 400Mbps for DDR/MDDR, up to 1066Mbps for LPDDR2/DDR2 and up to 2133Mbps for DDR3) applications with robust timing and small silicon area. The pre-assembled PHY contain everything you expect from a PHY: DDR I/Os, ESD, critical timing synchronization module (TSM) and a low jitter DLLs with fine-grain control. Optional light weight memory controller is available to support AHB/AXI and FIFO interface to CPU bus. Yes, we can customize the layout for you in one Micro.

MAIN FEATURES:

- Fully compatible with JEDEC LPDDR2/DDR/DDR2/DDR3 SDRAM,
- Low power, small area, scalable design
- Supports LPDDR2/DDR2/DDR3 speed grade up to 2133 Mbps, Ask if you need LPDDR3/DDR4
- SSTL_12, SSTL_15, SSTL_18 and SSTL_2
- Programmable output drive strength for power saving, support RDIMM or UDIMM
- Master and Slave DLLs for precise timing management with fine grade adjustment
- Accommodates industry standard x4, x8, x16 SDRAM widths and depths
- Lower power operation with optimal power management feature including deep power down
- Process, voltage and temperature drift compensation through Auto-calibration
- Embedded BIST logic for production test
- Optional PCB SI Simulation Service available
- Optional memory controller supports efficient AXI/AHB CPU bus and power saving modes
- Optimized look ahead command management to reduce system overhead
- 40nm/55nm/65nm/90nm/0.11/0.13um/0.18um process proven with test chip in SMIC/TSMC
- LPDDR3 and DDR4 solution coming soon!

BLOCK DIGRAM:



KEY ADVANTAGE:

- Easy to integrate, Fully pre-assembled PHY
- Low IO pin count
- 2 layer PCB supported
- Very High performance with low power modes
- Test chip and FPGA Integration Service available

APPLICATIONS:

- Mobile phones/PDAs/GPS
- Workstation/Server/PC/Laptop
- Portable storage devices
- High speed Switch/Router

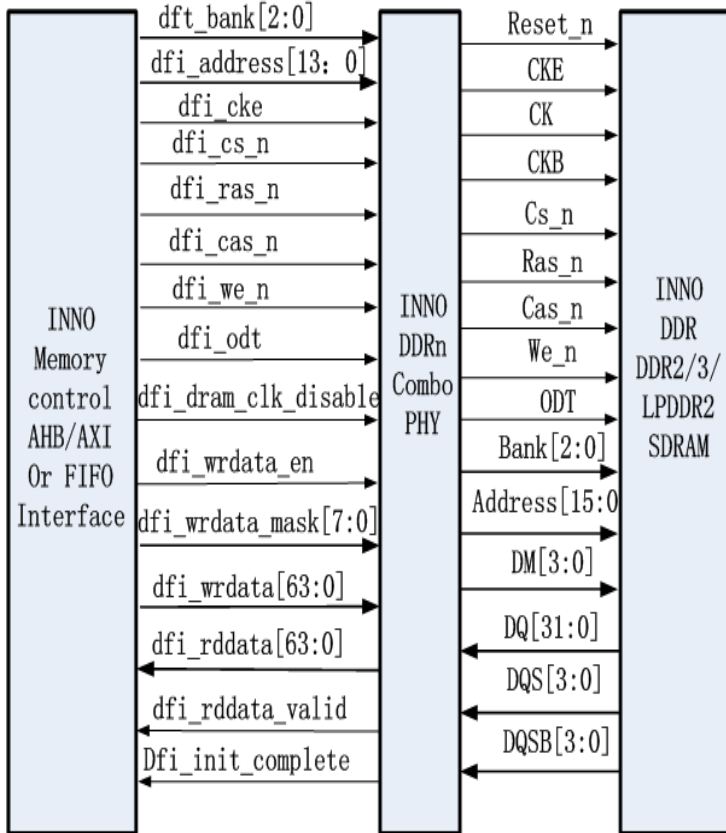
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Innosilicon LPDDR2/DDR2/DDR3 Combo PHY and Controller Turn Key IP Solution

DDR COMBO IP DATASHEET BRIEF

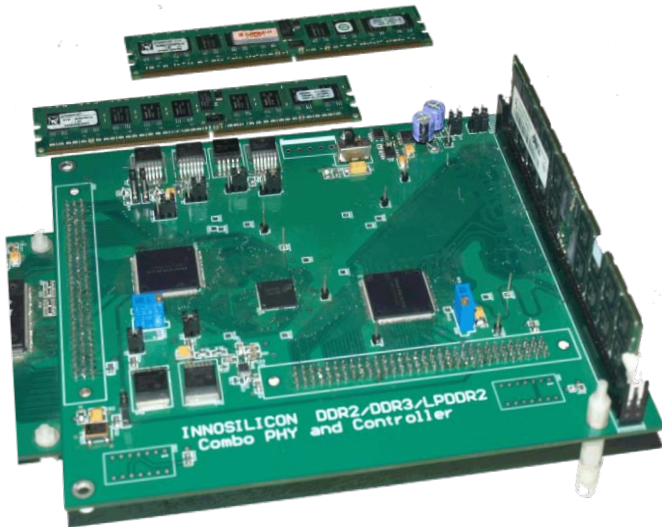
PHY CONTROLLER SYSTEM DIAGRAM:



SELECTED PHY PIN LIST (32 bit DQ Bus):

Pin name	Bits	IO	Function description
DQ	32	Bi	DQ Data
DQS/DQSB	8		Data Strobes
DM	4	O	Data Mask
BANK	3		Bank Address
ADDRESS	13		SDRAM Address
CS_n/RAS_n CAS_n/We_n	4		COMMAND
CK/CKB	1	I	differential Clock
dfi_address	13		Address
dfi_bank	2		Bank Address
dfi_cmd	4		dfi_cs_n,dfi_ras_n, dfi_cas_n ,dfi_we_n
dfi_cke	1		Clock Enable
dfi_odt	1		On Die Termination
dfi_wrdata_en			write enable
dfi_wrdata	64		write data
dfi_wrdata_m	8		write data mask
dfi_rddata_en	1		read data enable signal
dfi_rddata	64	O	read_data
dfi_rddata_valid	1		read_data_valid
Other signals

EVAL BOARD



DELIVERABLES:

- Data book and detailed physical implementation guides for the complete PHY including SSTL I/Os, Controller Interface Module and DLL Marcos
- Library Exchange Format (LEF)
- Full set of Timing Models
- Verilog Simulation Models
- FPGA Integration Support
- GDSII database for foundry merge
- Optional RTL memory controller Add-on
- Optional PCB layout SI simulation Services

Visit our website at www.innosilicon.com for additional product information.

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